CLAIM AMENDMENTS:

1. (Currently amended) A semiconductor device comprising:

a semiconductor chip;

first pads provided on a main surface of said semiconductor chip;

a light-receiving element portion provided on said main surface of said semiconductor chip such that a light-receiving surface thereof is exposed;

a light-transmitting portion provided so as to cover the light-receiving surface of said light-receiving element portion for transmitting incoming light to said light-receiving element portion;

an insulating film provided over said main surface of said semiconductor chip so as to expose surface portions of said first pads~~, the insulating film surrounding and contacting side surfaces of the first pads~~;

wiring patterns electrically connected to said first pads, the wiring patterns extending from said surface portions of said first pads and over said insulating film;

post portions provided on said wiring patterns~~, the post portions being electrically connected to the wiring patterns~~;

a sealing layer provided on said wiring patterns, on said insulating film, on a side surface of said light-transmitting portion, and on side surfaces of said post portions, such that an upper surface of said light-transmitting portion and top surfaces of said post portions are exposed, said sealing layer having cut side surfaces which are cut by a blade and which are substantially in the same plane of side surfaces of said semiconductor chip ~~the sealing layer surrounding a side surface of said light-transmitting portion~~; and

external terminals provided on the top surfaces of said post portions~~, the external terminals being electrically connected to said first pads via said wiring patterns~~.

2. (Withdrawn) A semiconductor device comprising:

a first semiconductor chip including a first main surface, a second main surface which opposes said first main surface and has a larger surface area than said first main surface, and side wall surfaces connecting said first main surface and second main surface;

first pads provided on the first main surface of said first semiconductor chip;

a light-receiving element portion provided on the first main surface of said first semiconductor chip such that a light-receiving surface thereof is exposed;

a light-transmitting portion provided so as to cover the light-receiving surface of said light-receiving element portion for transmitting incoming light to said light-receiving element portion;

a semiconductor chip carrying portion comprising a third main surface which includes a first region facing the second main surface of said first semiconductor chip and a second region which surrounds said first region, and a fourth main surface which opposes said third main surface;

a wiring layer which is electrically connected to said first pads and extends from said first pads, along said first main surface and said side wall surface, to said second region; and

external terminals which are provided over the second region and electrically connected to said first pads through said wiring layer.

3. (Withdrawn) A semiconductor device comprising:

a first semiconductor chip including a first main surface, a second main surface which opposes said first main surface and has a larger surface area than said first main surface, and side wall surfaces connecting said first main surface and second main surface;

first pads provided on the first main surface of said first semiconductor chip;

a light-receiving element portion provided on the first main surface of said first semiconductor chip such that a light-receiving surface thereof is exposed;

a light-transmitting portion provided so as to cover the light-receiving surface of said light-receiving element portion for transmitting incoming light to said light-receiving element portion;

a semiconductor chip carrying portion comprising a third main surface which includes a first region facing the second main surface of said first semiconductor chip and a second region which surrounds said first region, and a fourth main surface which opposes said third main surface;

a wiring layer which is electrically connected to said first pads and extends from said first pads, along said first main surface and said side wall surfaces, to said second region; and

external terminals provided over said fourth main surface side and electrically connected to said wiring layer via a conductive portion formed in a through hole which penetrates from the front to rear of said carrying portion.

4. (Withdrawn) The semiconductor device according to claim 3, wherein said light-transmitting portion is fixed in a position covering the light-receiving surface of said light-receiving element portion by a light-transmitting film serving as an adhesive layer, and

said light-transmitting film forms a sealing layer for burying and thereby sealing said first semiconductor chip.

5. (Withdrawn) The semiconductor device according to claim 3, wherein said light-transmitting portion is fixed in a position covering the light-receiving surface of said light-receiving element portion by a light-transmitting film serving as an adhesive layer which has a greater expansion coefficient than the expansion coefficient of said carrying portion,

a sealing layer for burying and thereby sealing said first semiconductor chip is provided on the lower side of said light-transmitting portion, and

said sealing layer on the upper side of said second region is formed by a sealing material having a smaller expansion coefficient than the expansion coefficient of said light-transmitting film.

6. (Withdrawn) The semiconductor device according to claim 3, wherein the surface area of a surface of said light-transmitting portion which opposes the light-receiving surface of said light-receiving element portion is formed to be greater than the surface area of the light-receiving surface of said light-receiving element portion, and

said light-transmitting portion comprises a convex portion and a concave portion provided on the periphery of said convex portion, said convex portion being disposed opposite said light-receiving surface and said concave portion being disposed opposite said wiring layer so as not to contact said wiring layer.

7. (Withdrawn) The semiconductor device according to claim 2, wherein said semiconductor chip carrying portion is set as a second semiconductor chip, and this second semiconductor chip is electrically connected to said wiring layer.

8. (Withdrawn) The semiconductor device according to claim 3, wherein said semiconductor chip carrying portion is set as a second semiconductor chip, and this second semiconductor chip is electrically connected to said wiring layer.

9. (Canceled).

10. (Previously presented) The semiconductor device according to claim 1, further comprising an oxidation film formed on the side surfaces of said post portions.

11. (Withdrawn) The semiconductor device according to claim 2, further comprising:

post portions provided between said wiring layer and said external terminals; and

a sealing layer provided on said wiring layer and on the side surfaces of said post portions,

wherein an oxidation film is formed on the side surface of said post portions.

12. (Canceled).

13. (Withdrawn) The semiconductor device according to claim 2, wherein a part of said wiring layer positioned on a boundary between said first main surface and said side wall surfaces is formed to be wider than the remaining parts of said wiring layer.

14. (Withdrawn) The semiconductor device according to claim 3, wherein a part of said wiring layer positioned on a boundary between said first main surface and said side wall surfaces is formed to be wider than the remaining parts of said wiring layer.

15. (Canceled).

16. (Currently amended) A semiconductor device comprising:

a semiconductor chip having a first main surface and a second main surface opposed to the first main surface;

a first pad formed on the first main surface;

a light-receiving element formed on the first main surface;

a light-transmitting member provided over said light-receiving element, [[the]] said light-transmitting member transmitting incoming light to said light-receiving element;

an insulating film provided over [[the]] said first main surface so as to expose surface portions of said first pad~~, the insulating film surrounding and contacting side surfaces of the first pad~~;

a wiring pattern electrically connected to said first pad, the wiring pattern extending from said surface portions of said first pad and over the insulating film;

a post electrode formed on the wiring pattern~~, the post electrode being electrically connected to the wiring pattern~~;

a sealing layer formed on said wiring pattern, on said insulating film, on a side surface of said light-transmitting member, and on a side surface of said post electrode, such that an upper surface of said light-transmitting member and a top surface of said post electrode are exposed, said sealing layer having cut side surfaces which are cut by a blade and which are substantially in the same plane of side surfaces of said semiconductor chip ~~the sealing layer surrounding a side surface of said light-transmitting member and~~; and

an external terminal formed on a top surface of said post electrode.

17. (Original) The semiconductor device according to claim 16, further comprising an oxidation film formed on the side surface of said post electrode.

18. (Previously presented) The semiconductor device according to claim 16, wherein the sealing layer directly contacts the side surface of said light-transmitting member.

19. (Previously presented) The semiconductor device according to claim 1, wherein the sealing layer directly contacts the side surface of said light-transmitting portion.

20. (New) The semiconductor device according to claim 16, wherein said wiring pattern physically and directly contacts said surface portions of said first pad.

21. (New) The semiconductor device according to claim 16, wherein said wiring pattern is uniformly spaced apart from said first main surface of said semiconductor chip.

22. (New) The semiconductor device according to claim 1, wherein said wiring patterns physically and directly contact said surface portions of said first pads.

23. (New) The semiconductor device according to claim 1, wherein said wiring patterns are uniformly spaced apart from said main surface of said semiconductor chip.